REMARKS/ARGUMENTS

Favorable reconsideration of this application as presently amended and in light of the following discussion is respectfully requested.

Claims 1-12 are presently active in this case. Claim 1 is amended and Claims 3-12 are added by the present amendment. Support for the amendment can be found at least at page 5, lines 19-25, page 13, lines 12-16, and page 17, lines 11-18, of the specification and at FIGs. 7 and 12.

In the outstanding Office Action, Claim 1 was objected due to informalities. Claim 1 is amended to correct these minor informalities. Accordingly, Applicants respectfully request the withdrawal of the objection to Claim 1.

Applicants and Applicants' representatives acknowledge with appreciation the courtesies extended to Applicants' representatives by Examiner Thanhha Pham during the personal interview conducted on October 28, 2004. During the personal interview, new Claims 4 and 7 as included herein were discussed. Further, amended Claim 1 includes features previously discussed within new independent Claims 4 and 7.

The outstanding Office Action also rejects Claims 1-2 under 35 U.S.C. § 102(e) as anticipated by Wu, et al. (U.S. Patent No. 6,730,556, herein "Wu"). For the reasons discussed below, Applicants respectfully traverse the art rejection.

Amended Claim 1 is directed to a semiconductor device including a first transistor and a second transistor. The first transistor includes a first gate electrode and a first sidewall insulating film formed on a side of the first gate electrode, and the second transistor includes a second gate electrode and a second sidewall insulating film formed on a side of the second gate electrode. Layers of insulating film of the second sidewall insulating film are more in number than layers of insulating film of the first sidewall insulating film. Accordingly, a

width of the second sidewall insulating film is greater than a width of the first sidewall insulating film. The first transistor also includes first source/drain active layers in electrical communication with first contacts, and the second transistor includes second source/drain active layers in electrical communication with second contacts. Further, the second source/drain active layers are formed at a distance from the second gate electrode greater than a distance of the first source/drain active layers from the first gate electrode.

In a non-limiting exemplary embodiment, FIG. 7 illustrates second source/drain active layers 9e, 9f formed at a distance from a second gate electrode 6a greater than a distance of the first source/drain active layers 9a, 9b from the first gate electrode 6b. FIG. 7 also illustrates first contacts 18a, 18d and second contacts 18b, 18c.

Wu describes an integrated circuit device 60 including a NMOS transistor 64 and a PMOS transistor 66. The NMOS transistor 64 includes a gate 84 and a region 92, and the PMOS transistor 66 includes a gate 104 and a region 132. The regions 92, 132 include HDD drain extensions 87/87', 107/107' and deep source/drain regions 90, 130 (See FIGs. 2d-2f and Col. 7, lines 20-25). The NMOS transistor 64 further includes insulating layers 88, 120 and the PMOS transistor 66 further includes insulating layers 120, 122', 128.

As shown in FIG. 2d, Wu teaches the formation of HDD regions 87, 107 at different distances D1N, D1P from their respective gates 84, 104 due to implantation around the spacers 120, 122'. Subsequently, an anneal is performed causing dopants within the HDD regions 87, 107 to migrate laterally, bringing the HDD regions 87', 107' to extend a comparable distance D2N, D2P under their respective gates, where D2N and D2P are *approximately the same dimension* (See FIG. 2e and Col. 5, line 66 – Col. 6, line 32). The differential lateral migration is achieved by using different dopants with different migration rates in HDD regions 87 and 107. Similarly, FIG. 2f and 2g illustrate the differential lateral

migration of differently-doped deep source/drain regions 90, 130 during annealing (Col. 6, line 55 – Col. 7, line 32). Annealing is performed to cause drain extension overlap OV1N to be *close to, or the same as*, OV1P (See Col. 7, line 33 – Col. 8, line 14). As discussed by Wu, equal overlaps OV1N and OV1P are desirable but not achieved by prior art methods (See Col. 7, lines 39-42).

During the personal interview, deep source/drain regions 90, 130 as illustrated in FIG. 2f were asserted as teaching Applicants' second source/drain active layers formed at a distance from the second gate electrode greater than a distance of the first source/drain active layers from the first gate electrode. However, it is respectfully noted that FIG. 2f illustrates an intermediate product of Wu's controlled overlap method. As the drain extension overlaps are not equal at this stage before annealing, it is respectfully submitted that Wu would have no intention of operating the device in this form, for example, by adding electrical contacts to the device for operation. In fact, the disclosure of Wu explicitly teaches away from using the device as illustrated in FIG. 2f because Wu describes that an equal drain extension overlap is desirable over an unequal overlap. Further, Applicants respectfully reiterate that Wu teaches different widths of insulating layers on the NMOS and PMOS transistors to ultimately arrive at equally-spaced extension regions 92, 132 by initially providing HDD regions 87, 107 and deep source/drain regions 90, 130 at different distances from the gates since these differently-doped regions 87, 107, 90, 130, migrate at different rates during annealing.

Additionally, FIG. 2g was also discussed during the personal interview. In this figure, the portions of the regions 92, 132 corresponding to the HDD regions 87', 107' were asserted as teaching Applicants' claimed features. Applicants respectfully note that FIG. 2g and Wu's teaching of controlled and equal overlap provides strong suggestion that these portions are not provided at different distances from their respective gates. Moreover, while Wu teaches

these portions of the gate extensions as extending beneath their respective gates, Wu is silent with regard to these portions extending *different distances* beneath their respective gates. Therefore, Wu does not teach or suggest all features of Applicants' amended Claim 1.

Accordingly, Applicants respectfully request the withdrawal of the art rejection based on Wu.

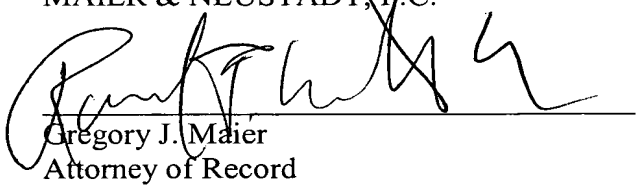
New independent Claims 4 and 7 are directed to a semiconductor device including a first transistor and a second transistor. Further, the device includes second source/drain active layers formed at a distance from a second gate electrode greater than a distance of first source/drain active layers from a first gate electrode. Claims 4 and 7 are considered allowable over the cited references for substantially the same reasons discussed above with regard to amended Claim 1.

Dependent Claims 3, 5-6, 8-9, and 10-12 are considered allowable for the reasons advanced for independent Claims 1, 4, and 7 from which they depend. These claims are further considered allowable as they recite other features of the invention that are not disclosed, taught, or suggested by the applied references or combination of references when those features are considered within the context of their corresponding independent base claims.

Consequently, in view of the above discussion, it is respectfully submitted that the present application is in condition for formal allowance, and an early and favorable reconsideration of this application is therefore requested.

Respectfully submitted,

OBLON, SPIVAK, McCLELLAND,
MAIER & NEUSTADT, P.C.



Gregory J. Maier
Attorney of Record
Registration No. 25,599

Raymond F. Cardillo, Jr.
Registration No. 40,440

Customer Number
22850

Tel: (703) 413-3000
Fax: (703) 413 -2220
(OSMMN 08/03)

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